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POWER ANALYSIS OF DIFFERENT FULL ADDER STRUCTURES USING ADIABATIC LOGIC

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Abstract— VLSI technology permits the designers to put additional variety of gates in a single IC. so as to realize the moveable VLSI primarily based application circuits the action of power optimization is important. In planning the complicated circuits like multipliers, dividers, modulators, the total adder could be a basic useful component in them. so as to get overall power improvement during a VLSI IC, the most aim is to cut back the facility consumption of the total adder. to style associate economical one bit full adder that is energy economical we have a tendency to are mistreatment the adiabatic logic here. The result of mistreatment the adiabatic logic is it neglects the quantity of exchange of energy with the encompassing atmosphere. Therefore the circuits that are designed mistreatment this logic can have negligible energy loss because of cooling.So it requires 28 transistors to get the true and complimentary arithmetic sum and carry output. The proposed adiabatic logic based full adder cell processes the three single bit inputs and provides the output as sum,carry,sum bar and carry bar in a single architecture. The proposed ALFA cell reduces the power consumption when compared to CMOS full adder.

Keywords— : Adiabatic Logic, CMOS Logic, energy dissipation, Full Adder, Low Power, Cache Memory, Arithmetic Operation, Leakage Power

I. INTRODUCTION

VLSI technology facilitates the designers for embedding more than hundred thousand of gates in a single IC. Achieving power reduction in full adder circuits is essential in handheld and portableVLSI based application circuits. Most of these application circuits incorporate processor-based blocks. Most probably, the circuits inside these blocks have full adder as their main element. Hence, in order to obtain the overall power optimization in a VLSI IC, as an initial attempt, the power reduction in full adders is the prime aim of the VLSI designers. Thus, in order to have an efficient approach, that is to implement the application circuits inside the VLSI. IC provide many choices for describing, synthesizing and verifying the designs with reduced complexity. Depletion of the silicon area during fabrication leads to the decline in power consumption. Thus, choosing low power consuming logic styles in the logical design stage and improving the efficiency of the physical design stage by adopting enhanced placement and routing techniques will yield a low power design with reduced propagation delay.

With this perception, the design and implementation of a low power full adder cell were carried out by selecting the low power consuming logic styles such as CMOS based 28T full adder cell, PTL based 16T full adder cell with TG, PTL based 14T full adder cell with TG and proposed ALFA cell. In VLSI, there is a trade- off between area, power and delay. To overcome these issues, it is necessary to design an optimized design. Hence the ALFA cell is proposed that overcomes the problems of the existing techniques such as CMOS Full Adder, PTL logic and transmission gate. The flow of this paper described full adder using various logic styles, elaborates the less area occupying and low power consuming efficient ALFA cell design approaches, the simulation outputs of the designed full adder cells with the considered logic styles are illustrated along with their respective area and power consumption results.

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to the another.

Logical Expression for SUM

= A' B' C-IN + A' B C-IN' + A B' C-IN' + A B C-IN

= C-IN (A' B' + A B) + C-IN' (A' B + A B')

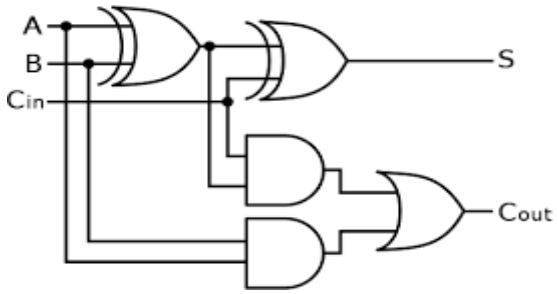
= C-IN XOR (A XOR B)= (1,2,4,7)

Logical Expression for C-OUT

= A' B C-IN + A B' C-IN + A B C-IN' + A B C-IN

= A B + B C-IN + A C-IN= (3, 5, 6, 7)

LOGIC DIAGRAM



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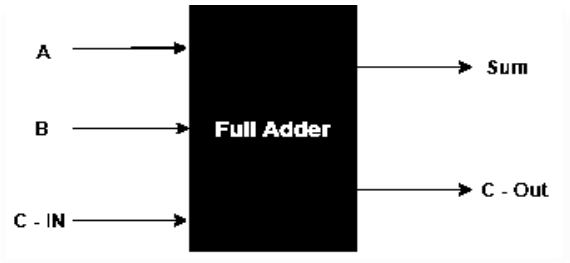
Block diagram



Truth table

A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Adiabatic logic circuits classified into two types: (a) Quasi/ Partial Adiabatic Logic Circuits (b) Full Adiabatic Logic Circuits

Quasi/Partial Adiabatic Logic Circuits

Quasi- adiabatic circuits have simple architecture and power clock system. The adiabatic loss occurs when current flows through non- ideal switch, which is proportional to the frequency of thepower- clock.

Popular Partially Adiabatic families include as:

i. Efficient Charge Recovery Logic(ECRL).
ii. 2N-2N2P AdiabaticLogic.
iii. Positive Feedback Adiabatic Logic(PFAL).
iv. NMOS Energy Recovery Logic-NERL.
v. Clocked Adiabatic Logic(CAL).
vi. True Single-Phase Adiabatic Logic(TSEL).
vii. Source-coupled Adiabatic Logic(SCAL).

Full Adiabatic Logic Circuits

Full-adiabatic circuits have no non-adiabatic loss, but they are much more complex than quasi-adiabatic circuits. All the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization.

Some Fully adiabatic logic families include:

(i) Pass Transistor Adiabatic Logic(PAL).

(**i**) Split-RailChargeRecoveryLogic(SCRL).

II LITERATURE SURVEY

Power dissipation is an increasing concern in VLSI circuits. New logic circuits have been developed to meet these power requirements. Power dissipation can be minimized by using various adiabatic logic circuits. In this paper an Adder circuit has been proposed based on 2PASCL and ECRL logic and then compared with Positive Feedback Adiabatic Logic(PFAL), Two-Phase Adiabatic Static Clocked Logic(2PASCL) respectively. Comparison shows significant power saving

Design of high performance and energy efficient digital systems are one of the most important research areas in VLSI system design which is suitable for real-time applications. One of the functional elements used in complex arithmetic circuits is an adder. To design an energy efficient adder one-bit full adder cell is designed based on adiabatic logic. The proposed ALFA cell is designed using adiabatic logic which results with the negligible amount of exchange of energy with the surrounding environment. Therefore, the application circuits based on this logic will have negligible energy loss due to heat dissipation

Full adder is the basic block of arithmetic circuit found in microcontroller and microprocessor inside arithmetic and logic unit (ALU). Improvement of the adder is thus essential for upgrade the performance of those circuits where adder is employed. Full adders, till now, have been designed using wide range of structures for improvement of various parameters like power consumption, speed performance and structure size. This paper described a comparative analysis of 28T and 14T full adder with the aim of increasing power efficiency and reducing structure size at 180nm technology. In this paper, the simulation results have been obtained for power by varying different parameters of the designed circuit using 180nm technology with Empyrean Aether

III EXISTING SYSTEM

Transmission gates are the fully restoring logic version of PTL whose output logic level does not degrade when passed throughthe respective logic level signal available on its inputs. Hence, in designing the full adder cells with PTL, in order to get the non- degraded outputs of the sum and carry, transmission gates are suitably inserted into the designs. PTL with TG based 16 transistors full adder cell is shown inFig. 1.The simulation results show that the PTL with TG based16T full adder cell has lower power consumption than that of the CMOS based 28T full addercell.

The PTL with TG based 14 transistors full adder cell is shown in figure 2. It has lower dynamic power consumption when compared, examine simple circuit configurations which can be used for adiabatic switching. A general circuit topology for the conventional CMOS gates and adiabatic counter parts is shown in Figure 3. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up transistor and the pull-down transistor networks must be replaced with complementary transmission- gate(T-gate).The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T- gate network implementing the pulldown function drives the complementary output node.

IV PROPOSED METHOD

NMOS Energy Recovery Logic(NERL)

NMOS energy recovery logic (NERL), which uses NMOS transistors only and as implement 6-phase clocked power. Its area overhead and energy consumption are smaller, compared with the other fully adiabatic logics. We employed boot strapped NMOS switches to simplify the NERL circuits. With the simulation results for a full adder, we confirmed that the NERL circuit consumed substantially less energy than the other adiabatic logic circuits at low-speed operation. NERL is more suitable than the other

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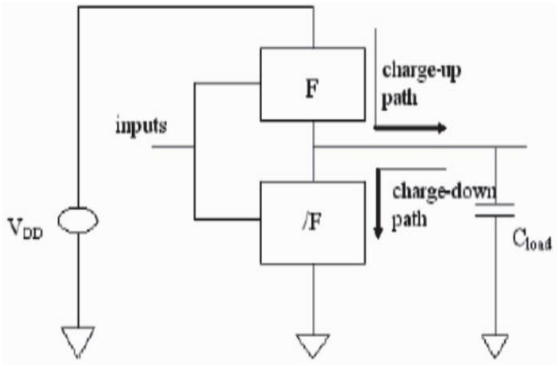
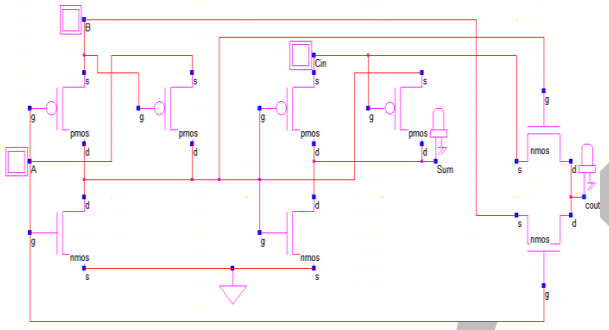
adiabatic logic circuits for the applications that do not require high performance but low energy consumption. NMOS energy recovery logic gate.

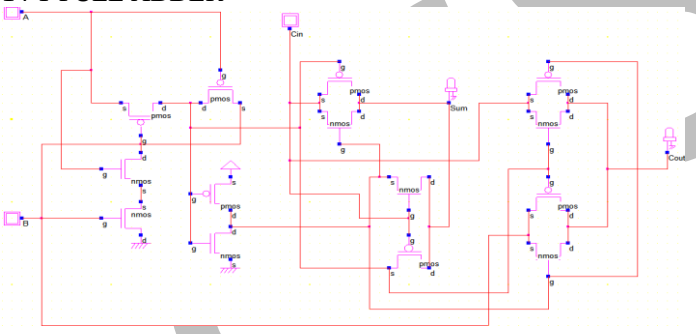


Logic diagrams of 8.14,24, and 28 transistor full adder circuits using adiabatic logic are shown below.

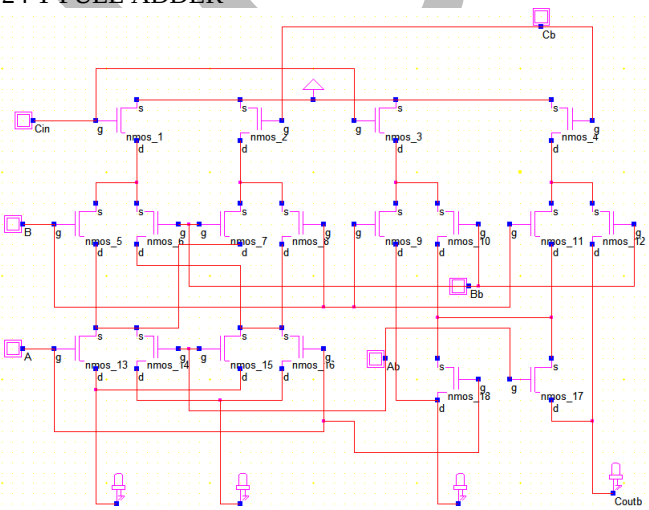
8 T FULL ADDER



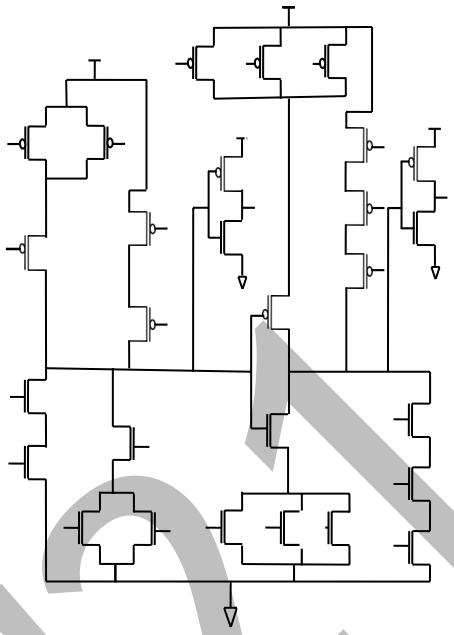
14 T FULL ADDER



24 T FULL ADDER



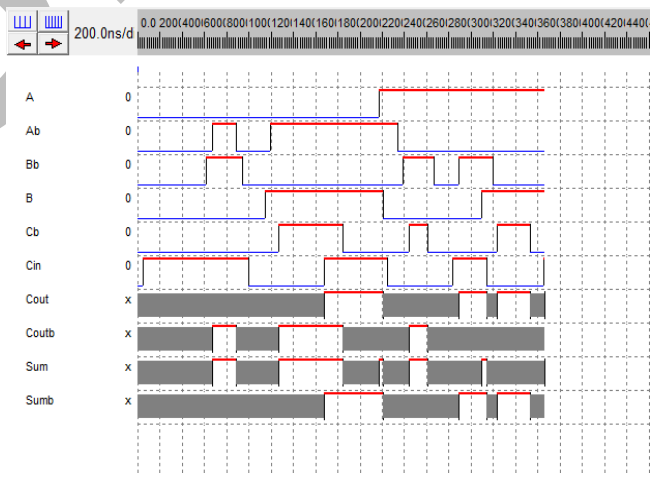
28 T FULL ADDER

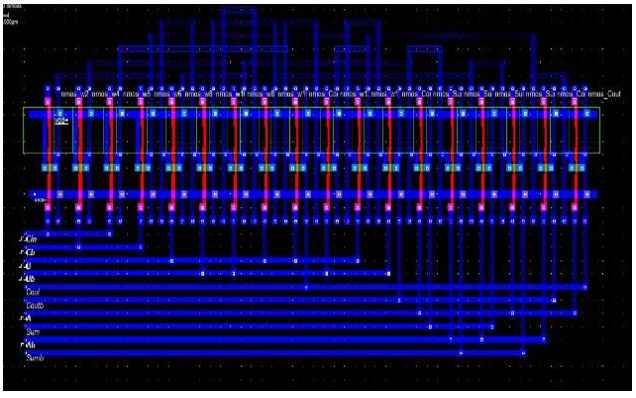


V.SIMULATION RESULTS

Following figure shows the Simulation wave form of 18 T FULL ADDER. Simulation 14 transistor, 24 transistor full adder and 28 transistor full adder circuits using adiabatic logic and their waveforms analysed.

14 T FULLADDER





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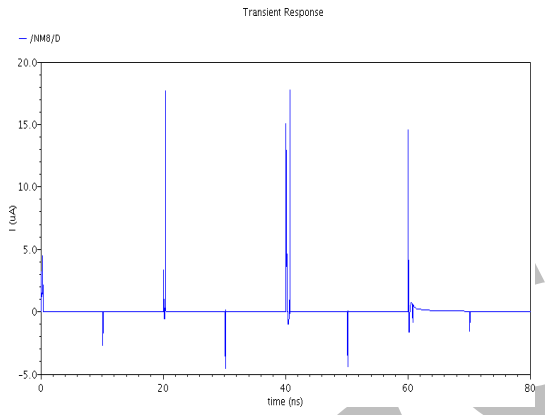
ANALYSIS OF POWER

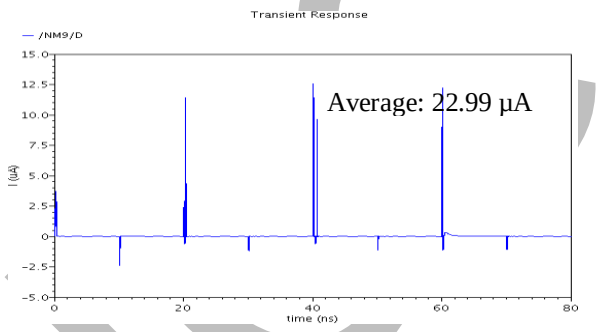
Output waveforms of various structures of full adder analysed and the power of 14 transistor and 28 transistor tabulated.

.Sr. No.	Parameter	28T Adder	14T Adder	14T Adder
1	Technology	180 nm	180 nm	180 nm
2	Supply	1 V	1 V	0.7
3	Power	78.21 µW	38.4 µW	21.04 µW
4	Reduction in structure size	69%	78%	78%

LEAKAGE CURRENT WAVE FORM OF 28 ALFA



LEAKAGE CURRENT WAVE FORM OF 14 ALFA



VI CONCLUSION

The ALFA cell has lower power consumption than that of the other versions of the full adder cell because of energy recycling. An ultra-power optimized ALFA cell is proposed using adiabatic logic with the aid of lower occupational area. The performance analysis of full adders in several logic designs is dispensed with the main target on getting optimized power consumption. The analysis in this paper has been carried out while analyzing both 14T and 28T full adders individually and comparing them on the basis of calculation of power by varying different parameters. The results show that 14T full adder has proved to be a better option as compared to 28T full adder, mostly in terms of power consumption. we observe that at 1.6 V, 28T adder consumes about 3 µW, while 14T consumes only 1.5 nW. Thus 14T consumes 10^3 times less power than the power consumed by 28T full adder.

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